METHOD FOR MAKING AN INTEGRATED OPTICAL CIRCUIT

Background Of The Invention

1. Field of the Invention

The present invention generally pertains to integrated optical circuits, and particularly to a method for manufacturing an integrated optical circuit.

2. Technical Background

Integrated optical circuits are usually constituted by optical and/or optoelectronic devices formed on a substrate. The optical and/or optoelectronic devices may be active devices (such as resonators, lasers, detectors, switches, etc.) or passive devices (such as waveguides, filters, couplers, etc.)

An interesting feature of integrated optical circuits resides in their compactness. However, these circuits experience optical losses as light propagates from one device to another on the substrate.

Light between the optical devices of an integrated circuit propagates through waveguides. Conventionally, waveguides are composed of a continuous structure made of a material having a higher refractive index than the surrounding substrate. Light propagates inside the waveguide by virtue of internal reflections off the faces thereof. Introduction of light into the waveguide is carried out so that the angle of reflection off the internal faces of the waveguide, as light propagates, is smaller than a critical angle depending on the refractive indices inside and outside the waveguide. This angle requirement may generally be fulfilled when the waveguide is in the form of a straight line. However, when the waveguide is bent (bent portions are needed in integrated

circuits in order to reduce their size), optical losses occur due to the fact that the reflection angle at the faces of the waveguide is too large, which gives rise to refractive waves.

One technique for reducing optical losses in integrated optical circuits, using a photonic crystal, consists in providing, around optical devices, a dielectric periodic structure which creates a frequency band gap. A frequency band gap is a range of frequencies (or photonic energy) at which propagation through the periodic structure is impossible. The parameters of the dielectric periodic structure, such as the period length, the refractive index of the structure, the shape of the periodic lattice, etc., are calculated so that the frequency of the light propagating inside the waveguides that interconnect the various optical circuits on the substrate is within the frequency band gap. Thus light remains confined inside the optical circuits and waveguides since it cannot radiate outside these optical devices, in the dielectric periodic structure.

Figure 1 illustrates an example of such an integrated optical circuit. For the purpose of simplification, the integrated optical circuit of Figure 1 essentially consists of a waveguide 1 surrounded by a dielectric periodic structure 2. The waveguide 1 receives light on one lateral side thereof as shown by arrow 3. Light propagates inside the waveguide to emerge from the other lateral side as shown by arrow 4.

The integrated circuit comprises a substrate 5 coated with a dielectric layer 6 having a higher refractive index than the substrate 5. The dielectric periodic structure 2 is arranged along the longitudinal sides of the waveguide 1. The structure 2 typically consists of an array of holes 2a formed throughout the layer 6 and substrate 5, perpendicularly to the longitudinal axis of the waveguide 1, but, as a variant, may also consist of an array of rods. The waveguide 1 is defined by the central portion of the dielectric layer 6 bounded by the periodic structure 2. Horizontal radiation of light out of the longitudinal sides of the waveguide 1 is prevented by the periodic structure 2, which reflects, according to a diffraction phenomenon, optical waves having frequencies within the corresponding band gap. Light is further vertically confined within the waveguide by virtue of the fact that the refractive index of the waveguide is higher than that of the substrate 5 and that of air. Alternatively, it is also possible to provide a three-dimensional dielectric periodic structure around the waveguide, instead

of the two-dimensional structure as illustrated in figure 1, in order to confine the light within the waveguide both horizontally and vertically.

Summary Of The Invention

The present invention provides a reliable method for manufacturing an integrated optical circuit in which an optical device, such as a waveguide, a resonator, etc., is associated with an optical structure, such as an array structure defining a frequency band gap region. Both the optical device and the optical structure may be formed with great accuracy.

The method generally comprises the steps of: forming a first mask on a face of a substrate, the first mask defining a pattern corresponding to at least one optical device to be formed in a first region of the substrate; forming a second mask on the face of the substrate, the second mask defining a pattern corresponding to an optical structure to be formed in a second region of the substrate, distinct from the first region; and etching the substrate having thereon the first and second masks, in order to form the at least one optical device and the optical structure in the substrate.

By virtue of the simultaneous use of the first and second masks, each one corresponding to a region of the substrate, it becomes possible to form the optical device(s) and the optical structure(s) on the substrate in a simple manner and with great accuracy.

A reason for this is that the two masks may be formed separately and, therefore, two respective specific patterning methods may be applied to form the two masks. In other words, the patterning technique used to form the second mask, corresponding to the second region of the substrate, may be different from that used to form the first mask, corresponding to the first region of the substrate.

This is particularly important, especially in the context of photonic crystals, when it is desired to manufacture integrated optical circuits having one or more optical devices, such as waveguides, couplers, etc., and an array structure defining a photonic band gap proximate to the optical device(s). Indeed, in such a case, the optical device(s) and the array structure have quite different shapes. The array structure to be formed in the substrate is periodic or quasi periodic, with a period which may be small, in the order of 250-500 nm. The construction of this periodic structure requires a

specific technique suitable for forming a mask with small irregularities, such as holes, disposed according to a periodic lattice. A typical such technique may consist of interference or holographic lithography, which uses two interfering laser beams irradiating the wafer. Interference lithography however is not appropriate for forming a mask corresponding to the optical devices (waveguides, resonators, couplers...), because these devices generally do not consist of a periodic or quasi periodic structure. A conventional lithography technique employing UV (ultra-violet) exposure will, on the contrary, enable such a mask to be satisfactorily formed. Thus, the present invention makes it possible to select, for each of the first and second regions of the substrate, a specific appropriate patterning technique for forming the corresponding mask.

By contrast, using a single mask for both the optical device(s) and the optical structure would require, in many cases, a complicated lithography method for producing the mask, namely a method which would be adapted to all kinds of shape contained in the pattern to be created in the substrate. The known UV or electron beam exposure lithography techniques, although suitable for producing masks corresponding to optical devices such as waveguides, lasers, etc., cannot offer, for the time being, a sufficient accuracy for forming frequency band gap structures.

Another advantage of the present invention resides in that the two masks are used simultaneously, so as to form the optical device(s) and the optical structure together. The present invention thus provides a simple process, requiring only one etching step for the substrate.

Preferably, the method according to the invention further comprises the step of removing the first and second masks.

The step of etching the substrate may consist of a dry etching step using a predetermined etching gas, for example a fluorine-bearing gas such as SF_6. In this case, the first and second masks are each made of a material which substantially resists the predetermined etching gas.

Preferably, in order to simplify the manufacturing method, the step of forming the first mask and the step of forming the second mask are carried out in such a manner that one of the first and second masks overlays the other. There is then no need to define two separate zones where, respectively, the first and second masks have to be

formed, since one of the two masks may overlay the other. In practice, one of the first and second masks has a first portion which overlays the other mask and a second portion which is in direct contact with the substrate.

According to the invention, one of the first and second masks may be formed using an interference lithography technique, whereas the other may be formed using a UV exposure technique.

Advantageously, the second mask is formed by carrying out an interference lithography technique, and the first mask is made of a material which is substantially insensitive to the radiation used in the interference lithography technique, so that the second mask may be formed after the formation of the first mask without affecting the first mask.

The step of forming the second mask may then comprise the steps of: forming a photoresist layer on the face of the substrate supporting the first mask, and forming the pattern corresponding to the optical structure in the photoresist layer using the interference lithography technique.

According to a first embodiment of the present invention, the first and second masks are respectively made of metal and a photoresist material. The metal may typically consist of at least one of the following metals : nickel, chromium and gold.

According to this first embodiment, the step of forming the first mask comprises the steps of : forming a first layer on the substrate, the first layer being made of a material which is substantially insensitive to light ; forming a photoresist layer on the first layer ; patterning the photoresist layer using a UV exposure technique, so as to obtain a photoresist pattern corresponding to the first region of the substrate ; etching the first layer using the photoresist pattern as a mask ; and removing the photoresist pattern.

The above-mentioned step of etching the first layer may consist of a wet etching step.

According to a second embodiment of the present invention, the first and second masks are both made of a photoresist material, the first mask being however constituted by a photoresist material which has been heated in order to remove its sensitivity to light.

According to this second embodiment, the step of forming the first mask comprises the following steps : forming a photoresist layer on the substrate ; patterning the photoresist layer using a UV exposure technique, so as to obtain a pattern corresponding to the first region of the substrate ; and heating the photoresist pattern in order to remove its sensitivity to light.

According to a third embodiment of the present invention, the first mask is formed using a UV exposure technique, and the second mask is made of a material which is substantially insensitive to UV, so that the first mask may be formed after the formation of the second mask without affecting the second mask.

In this third embodiment, the step of forming the second mask comprises the steps of : forming a first layer on the substrate, the first layer being made of the material which is substantially insensitive to UV ; forming a photoresist layer on the first layer ; patterning the photoresist layer using an interference lithography technique, so as to obtain a photoresist pattern corresponding to the second region of the substrate ; etching the first layer using the photoresist pattern as a mask ; and removing the remaining photoresist pattern.

The step of forming the first mask then comprises the steps of : forming a photoresist layer on the second mask, and forming the pattern corresponding to the at least one optical device in the photoresist layer using the UV exposure technique.

The substrate used in the three embodiments above is preferably a silicon on insulator substrate.

The optical structure formed in the substrate typically consists of an array structure proximate to the optical device. In practice, the integrated optical circuit as obtained by the method according to the invention may comprise a waveguide, as the optical device, and an array structure having a frequency bandgap, as the optical structure. The array structure may take the form of a periodic array of holes or a periodic array of rods.

Brief Description Of The Drawings

Figure 1 is a perspective view showing a known integrated optical circuit;

Figures 2A to 2J are section views diagrammatically showing a method for manufacturing an integrated optical circuit according to a first embodiment of the present invention;

Figure 3 is a perspective view showing an integrated optical circuit with an array of holes obtained by the method according to the first embodiment of the invention;

Figure 4 is a perspective view showing an integrated optical circuit with an array of rods obtained by the method according to the first embodiment of the invention;

Figures 5A to 5H are section views diagrammatically showing a method for manufacturing an integrated optical circuit according to a second embodiment of the present invention; and

Figures 6A to 6F are section views diagrammatically showing a method for manufacturing an integrated optical circuit according to a third embodiment of the present invention.

Detailed Description Of Preferred Embodiments

Figures 2A to 2J diagrammatically show a method for manufacturing an integrated optical circuit according to a first embodiment of the invention. For the purpose of simplification, the method illustrated in figures 2A to 2J is directed to the manufacture of a waveguide surrounded by an array structure. However, optical devices other than waveguides may be produced by the method according to this first embodiment.

At a first step (figure 2A), a metal layer 8 and a photoresist layer 9 are successively formed on a substrate 7. The substrate 7 is preferably a silicon on insulator (SOI) substrate, i.e. a substrate composed of a silicon base substrate 7a, coated with a thin silica layer 7b which in turn is coated with a thin silicon layer 7c. The silicon layer 7c has a higher refractive index than the silica layer 7b, for reasons which will be explained below. The metal constituting the layer 8 may consist, for example, of nickel, chromium or gold.

At a second step (figure 2B), a silica mask 10 is applied onto the photoresist layer 9, in a manner known to the skilled person. The silica mask 10 supports, on a portion of its upper surface, a chromium pattern 10a taking the shape of the optical waveguide to be formed in the substrate 7, namely, in the embodiment as illustrated in

figure 2B, the shape of a strip. The chromium pattern 10a is located on the upper surface of the silica mask 10 so as to face a region 7d of the silicon layer 7c where the optical waveguide is to be formed. The wafer 7, 8, 9 as shown in figure 2B is then exposed to UV radiation through the silica mask 10. The portions of the silica mask 10 which are not covered by the chromium pattern 10a are transparent to UV. The chromium pattern 10a, on the contrary, reflects UV light and therefore prevents a region 9a of the photoresist layer 9 situated below the pattern 10a to be exposed.

At a third step (figure 2C), the silica mask 10 is removed and the photoresist 9 is developed. Development of the photoresist 9 results in removal of the portions thereof which have been exposed to UV light. At the end of the third step, only a portion 9a of the photoresist layer 9, having the same shape as the chromium pattern 10a and the optical waveguide to be formed, remains on the metal layer 8.

At a fourth step (figure 2D), the metal layer 8 is wet etched, using the photoresist portion 9a as a mask, thereby forming a metal pattern or mask 8a on the substrate 7. Wet etching of the metal layer 8 is carried out by means of an appropriate acid capable of attacking the metal while leaving the photoresist mask 9a substantially unaffected. Examples of such an acid may be the commercially available Gold-Etch (registered trade mark) acid, when the metal is gold, and Nickel-Etch (registered trade mark) acid, when the metal is nickel. The photoresist mask 9a is then removed using a solvent (figure 2E).

At a fifth step (figure 2F), a photoresist layer 11 is formed on the substrate 7 and the metal mask 8a, so that the metal mask 8a is sandwiched between the thin silicon layer 7c of the substrate and the photoresist layer 11. More specifically, a portion of the layer 11 directly covers the upper face 7e of the substrate while another portion covers the metal mask 8a which is formed on the upper face 7e. The portion of the layer 11 which is in direct contact with the face 7e corresponds to a region of the substrate 7, denoted by reference numeral 7f in figure 2F, where the array structure is to be formed.

At a sixth step (figure 2G), two interfering laser beams 12 are directed towards the wafer to expose the photoresist layer 11 to a light interference pattern. The interfering laser beams 12 are arranged in such a manner that, after development of the photoresist layer 11 (figure 2H), the latter defines a pattern 11a in the form of a periodic array of holes. Due to the fact that the mask 8a is made of a material, i.e. metal, which

is substantially insensitive to light, the formation of the pattern 11a may be carried out without affecting the mask 8a. Thus, at the end of the sixth step, the substrate 7 supports a first mask 8a and a second mask 11a, which are respectively associated with the regions 7d and 7f of the substrate 7 where the waveguide and the array structure are to be formed. The two masks 8a, 11a are made of different materials, i.e. metal for the first mask and photoresist for the second mask. Both of these materials are able to resist the dry etching step that is described below.

At a seventh step (figure 2I), the substrate 7, and more particularly the silicon layer 7c, is dry etched. To this effect, the wafer 7, 8a, 11a is placed in a plasma chamber containing a process gas, and a plasma is generated inside the chamber from the process gas. The plasma includes reactive species which are able to selectively etch the silicon layer 7c, i.e. without eroding the first and second masks 8a, 11a. Typically, the process gas may contain a fluorine-bearing etching gas such as SF_6.

At an eight step (figures 2J), the first and second masks 8a, 11a are removed by appropriate solvents. The integrated optical circuit as obtained is constituted by the silicon base substrate 7a, the silica layer 7b, a waveguide 12 and a periodic array of holes 13. The periodic array of holes 13 has a frequency band gap which prevents horizontal radiation of light from the inside to the outside of the waveguide 12. Light propagating inside the waveguide 12 is further confined vertically by virtue of the fact that the waveguide exhibits a higher refractive index than the silica layer 7b. The integrated optical circuit as diagrammatically shown in figure 2J, in section view, is represented in perspective in figure 3.

As a variant to the integrated optical circuit as illustrated in figures 2J and 3, the circuit obtained by the method according to the present invention may have an array structure which consists of a periodic array of rods, instead of holes. Figure 4 shows such an alternative result. In figure 4, the same elements as in figures 2J and 3 are designated by the same reference numerals. Thus, the integrated optical circuit of figure 4 comprises a base substrate 7a, a silica layer 7b, a waveguide 12 and a periodic array of rods 13' formed in the silicon layer 7c. With respect to the integrated circuit as shown in figures 2J and 3, the circuit of figure 4 may be achieved by merely executing the dry etching step (seventh step above) for a longer time.

Figures 5A to 5H diagrammatically show a method for manufacturing an integrated optical circuit according to a second embodiment of the invention. For the purpose of simplification, the method illustrated in figures 5A to 5H is directed to the manufacture of a waveguide surrounded by an array structure. However, optical devices other than waveguides may be produced by the method according to this second embodiment.

At a first step (figure 5A), a photoresist layer 15 is formed on a substrate 14. The substrate 14 is preferably a silicon on insulator (SOI) substrate, i.e. a substrate composed of a silicon base substrate 14a, coated with a thin silica layer 14b which in turn is coated with a thin silicon layer 14c. The thin silicon layer 14c has a higher refractive index than the thin silica layer 14b, for the same reasons as in the first embodiment.

At a second step (figure 5B), a silica mask 16 bearing a chromium pattern 16a is laid on the photoresist layer 15. The chromium pattern 16a is located on the upper surface of the silica mask 16 so as to face a region 14d of the silicon layer 14c where the optical waveguide is to be formed. Then the wafer 14, 15 is exposed to UV radiation through the mask 16, in the same manner as in the second step of the first embodiment.

At a third step (figure 5C), the silica mask 16 is removed and the photoresist layer 15 is developed. The result thereof is the removal of all the portions of the layer 15 which were exposed to UV radiation during the second step. At the end of this third step, only the portion of the photoresist layer 15 located below the chromium pattern 16a remains on the substrate 14, thus defining a photoresist pattern 15a on the substrate. The photoresist pattern 15a faces the region 14d of the silicon layer 14c where the optical waveguide is to be formed.

At a fourth step (not shown), the photoresist pattern 15a is heated in order to remove, or at least greatly reduce, its sensitivity to light. This step is carried out by placing the wafer 14, 15a into a furnace, and by baking it at about 180°C for approximately half an hour. The photoresist pattern 15a obtained after this fourth step will be referred to hereinafter as "first mask 15a".

At a fifth step (figure 5D), another photoresist layer 16 is deposited on the substrate 14 and the first mask 15a, so that the first mask 15a be sandwiched between

the thin silicon layer 14c of the substrate and the photoresist layer 16. More specifically, a portion of the layer 16 directly covers the upper face 14e of the substrate while another portion covers the first mask 15a which is formed on the upper face 14e. The portion of the layer 16 which is in direct contact with the face 14e corresponds to a region of the substrate 14, denoted by reference number 14f in figure 5D, where the array structure is to be formed.

At a sixth step (figure 5E), two interfering laser beams 17 are directed towards the wafer to expose the photoresist layer 16 to a light interference pattern. The interfering laser beams 17 are arranged in such a manner that, after development of the photoresist layer 16 (figure 5F), the latter defines a pattern 16a in the form of a periodic array of holes. Due to the fact that the first mask 15a was made insensitive to light at the fourth step, the formation of the pattern 16a may be carried out without affecting the first mask 15a. Thus, at the end of the sixth step, the substrate 14 supports the first mask 15a and a second mask 16a, which are respectively associated with the regions 14d and 14f of the substrate 14 where the waveguide and the array structure are to be formed. Both of the first and second masks are made of a material which is able to resist the dry etching step that is described below.

At a seventh step (figure 5G), the substrate 14, and more particularly the thin silicon layer 14c, is dry etched. To this effect, the wafer 14, 15a, 16a is placed in a plasma chamber containing a process gas, and a plasma is generated inside the chamber from the process gas. The plasma includes reactive species which are able to selectively etch the silicon layer 14c, i.e. without eroding the first and second masks 15a, 16a. Typically, the process gas may contain a sulphur-bearing etching gas such as SF_6.

At an eighth step (figures 5H), the first and second masks 15a, 16a are removed by appropriate solvents. The integrated optical circuit as obtained is constituted by the silicon base substrate 14a, the silica layer 14b, a waveguide 18 and a periodic array of holes 19. Instead of the periodic array of holes 19, a periodic array of rods may be formed by executing the dry etching step for a longer time.

Figures 6A to 6F diagrammatically show a method for manufacturing an integrated optical circuit according to a third embodiment of the invention. For the purpose of simplification, the method illustrated in figures 6A to 6F is directed to the

manufacture of a waveguide surrounded by an array structure. However, optical devices other than waveguides may be produced by the method according to this third embodiment.

The method according to this third embodiment differs from the first embodiment notably in that the second mask, corresponding to the optical structure, is formed prior to the formation of the first mask, corresponding to the optical waveguide. Furthermore, the second mask is made of metal, whereas the first mask is made of a photoresist material.

More specifically, the second mask, denoted by reference numeral 21a, is formed by depositing a metal layer 21 on a SOI substrate 20 (figure 6A), depositing a photoresist layer 22 on the metal layer 21, patterning the photoresist layer 22 using an interference lithography technique so as to define therein a photoresist pattern 22a (figure 6B), and wet etching the metal layer 21 through the photoresist pattern 22a (figure 6C). The first mask, denoted by reference numeral 23a, is formed after removal of the remaining photoresist pattern 22a (figure 6D) by depositing a photoresist layer 23 on the second mask 21a (figure 6E), exposing the wafer to UV through a silica mask 24 having a chromium strip 24a, and developing the photoresist 23 so as to define a pattern 23a corresponding to the optical waveguide (figure 6F). The etching step for etching the silicon layer 20c of the substrate 20 is identical to that performed in the first and second embodiments.

The third embodiment as described above has the advantage that the position of the first mask 23a on the second mask 21a may be accurately selected using the holes of the second mask 21a as references when laying the silica mask 24 on the photoresist layer 23 as shown in figure 6E.

The first, second and third embodiments as described above are preferred embodiments for the present invention. However, it will be clearly apparent to the skilled person that the present invention may be carried out differently without departing from the scope of the appended claims. In particular, the SOI substrate used in these embodiments could be replaced, for example, by a substrate composed of a glass base substrate coated with a silicon layer.

Furthermore, the present invention is not limited to the manufacture of integrated optical circuits having a periodic array of holes or rods. The present

invention could indeed be used for forming, in a same substrate, optical devices associated with Bragg reflectors. In a general manner, the method according to this invention may be applied when different optical devices or structures are to be formed in a substrate, and is particularly advantageous when the the optical devices or structures exhibit quite different shapes, requiring the use of different patterning techniques for producing the corresponding masks.